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A Hybrid Approach for Mitigating Transient and Permanent Faults in Memory Subsystems Using EDC, ECC, and BIST

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I.ABSTRACT

A fault-tolerant 64×16 Random Access Memory (RAM) architecture has been designed and validated using Verilog HDL, supported by a comprehensive System Verilog-based verification environment. The system incorporates both Error Correction Code (ECC) and Built-In Self-Test (BIST) mechanisms to increase reliability and maintain data integrity in environments susceptible to transient and permanent faults—making it suitable for safety-critical and high-dependability applications. The ECC module implements a Hamming SEC–DED (Single Error Correction, Double Error Detection) scheme, generating five parity bits for every 16-bit input, resulting in a 21-bit encoded output. During read operations, the ECC decoder computes the syndrome to correct single-bit errors and detect double-bit errors. The BIST controller enables autonomous memory testing by writing predefined patterns, reading them back, and comparing results to identify permanent faults, thereby removing the need for external test hardware. The top-level architecture integrates the RAM array, ECC encoder/decoder, and BIST controller, supporting seamless switching between normal operation and self-test modes. Extensive verification using System Verilog testbenches—covering fault injection and random stimulus testing—confirms the system's ability to accurately detect and correct memory errors, demonstration strong robustness in fault-prone operating conditions.

II.INTRODUCTION

Memory serves as a critical building block in System-on-Chip (SoC) architectures, providing the essential storage and data-

handling capabilities required for modern digital systems. Most SoC designs incorporate embedded memory blocks, commonly implemented using Static Random Access Memory (SRAM) because of its high-speed operation and easy integration with digital logic. However, SRAM requires more silicon area, which negatively impacts power efficiency and manufacturing yield. On the other hand, Dynamic Random Access Memory (DRAM) uses capacitor-based storage cells, allowing a much smaller area footprint. The drawback is that DRAM must be periodically refreshed to retain data, adding both design complexity and extra power consumption. SRAM, built from flip-flop structures, eliminates the need for refresh cycles and delivers faster access times than DRAM. Nevertheless, its larger area limits scalability in compact or resource-constrained designs. Single-port RAM is a simpler and more area-efficient memory option, but it supports only one access per clock cycle, which restricts performance in high-bandwidth applications. Dual-port RAM overcomes this limitation by enabling simultaneous access to different memory locations, resulting in significantly enhanced throughput.

III.LITERATURE SURVEY

Transparent BIST for ECC-Based Memory Repair, Michael Nicolaidis, Panagiota Papavramidou 2013 This paper proposes a BIST approach compatible with ECC-equipped memory systems. It allows in-field, transparent testing without affecting normal ECC operation. The architecture uses a smart repair algorithm that integrates seamlessly with ECC. It enables fault detection and correction for permanent and transient faults. This method is especially useful for embedded and safety-critical applications. It reduces system downtime while enhancing memory reliability.

A Memory Yield Improvement Scheme Combining BIST and ECC, Tze-Hsin Wu, Po-Yuan Chen, Mincent Lee, Min-Jer Wang ,2012. The study proposes ECC-Enhanced Memory Repair (EEMR) to improve manufacturing yield. EEMR combines ECC with Built-In Redundancy Analysis (BIRA) in a sequential repair process. It analyzes different ECC configurations and fault distributions in memory arrays. Over 2% improvement in yield was observed in 100,000 memory instances. The scheme adapts to various defect patterns effectively. It is efficient for large-scale memory arrays in commercial systems.

Evaluating Built-in ECC of FPGA On-Chip Memories for Fault Mitigation Behzad Salami, Osman Unsal, Adrian Cristal 2019. This paper evaluates ECC's effectiveness in FPGA BRAMs under voltage under scaling. Results show that built-in SEC-DED ECC handles over 90% of under volting faults. Additional 7% of faults are detected (but not corrected), improving robustness. It applies to neural

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accelerators with 40% power savings and minor accuracy loss. The work highlights ECC's role in energy-efficient fault tolerance. It supports ECC as a reliable method for transient error correction in FPGAs.

IV. PROPOSED IMPLEMENTATION

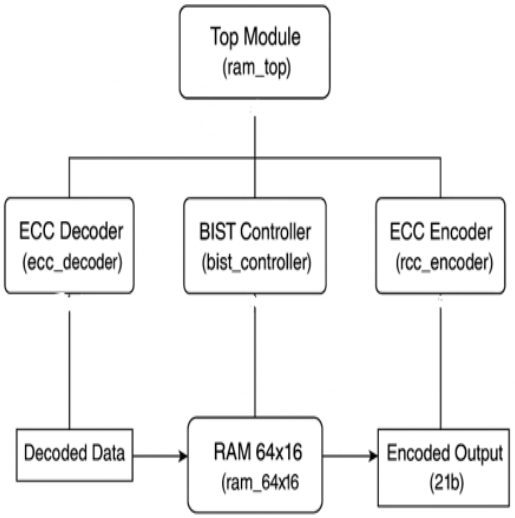

Fig:1 BLOCK DIAGRAM

The image illustrates a block diagram of a RAM system integrated with Error Correction Code (ECC) and Built-In Self-Test (BIST) functionality. At the top level, the ram_top module coordinates the operation of all submodules. Three primary components interface directly with this top-level module: the ECC Decoder, the BIST Controller, and the ECC Encoder. The ECC Decoder processes data read from memory, performing error detection and correction before outputting the corrected 16-bit data. The BIST Controller manages the autonomous testing of the RAM, ensuring the detection of permanent faults without external test equipment. The ECC Encoder generates the necessary error-correcting bits and outputs the encoded 21-bit data during write operations. All submodules interact with the core memory block, labelled RAM 64×16 (ram_64x16). Data flows from memory to the ECC Decoder for correction, while outgoing data passes through the ECC Encoder for protection. This architecture enhances both data reliability and overall system testability.

RESULTS

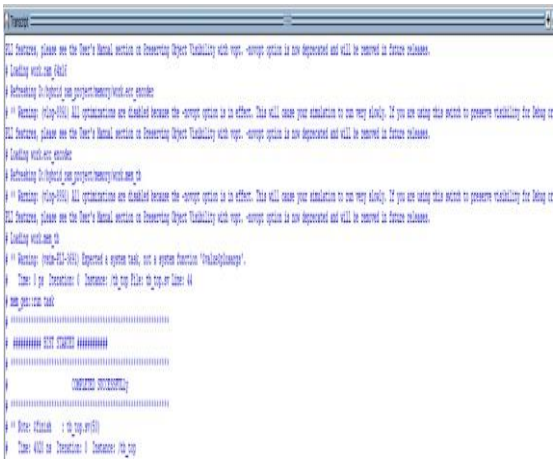

Fig: 2(a) write and read operations

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```
# mem_gen::run task
#############****ACTUAL DATA = 2286 *********#########
#############****ERROR DATA  = 2287 *********#########
# ****************************************************
# printing = mem_tx
# addr          = 30
# data          = 2287
# wr_rd         = 1
# err_inst = x
# bist_start= 0
# ****************************************************
# ****************************************************
# printing = mem_tx
# addr          = 30
# data          = 2286
# wr_rd         = 0
# err_inst = x
# bist_start= 0
# ****************************************************
# ** Note: $finish    : tb_top.sv(50)
#    Time: 4020 ns  Iteration: 0  Instance: /tb_top
# 1
# Break in Module tb_top at tb_top.sv line 50
```

Fig: 2 (b)write and read operations

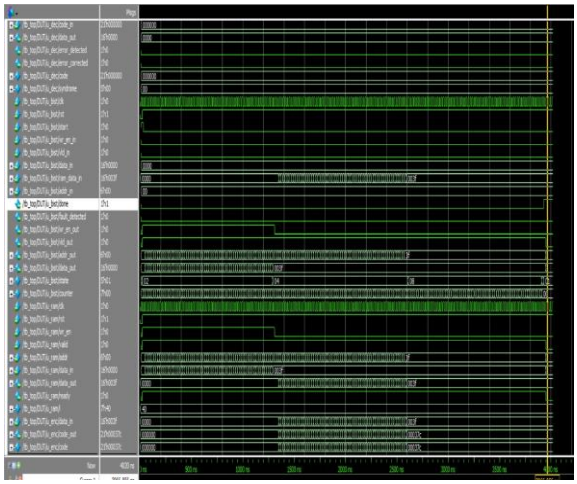

Fig: 3(a) wave form simulation

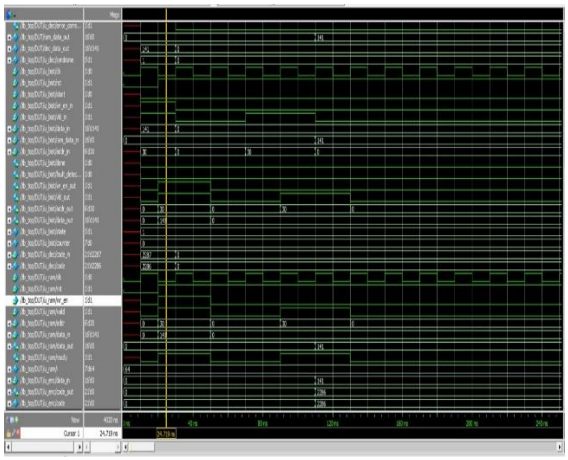

Fig: 3(b) wave form simulation

CONCLUSION

The design and verification of the 64×16 fault-tolerant RAM system demonstrate a robust solution for protecting data against both transient and permanent faults. By incorporating Hamming SEC–DED–based Error Correction Code (ECC) and a Built-In Self-Test (BIST) controller, the architecture provides dependable error detection, correction, and self-diagnostic capabilities. The ECC module performs real-time single-bit error correction and double-bit error detection, while the BIST controller conducts autonomous fault testing without the need for external test equipment. The support for dual operating modes—normal operation and self-test—adds flexibility for continuous fault monitoring and management. Extensive functional verification using a System-Verilog testbench, including targeted fault injection scenarios, validated the system's reliability and behavior under various fault conditions. This architecture is highly suitable for safety-critical and mission-critical environments such as aerospace, automotive, industrial automation, and other domains where uncompromised reliability is essential.

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